# NI PXI/PCI-5122 Specifications

#### 14-Bit 100 MS/s Digitizer

Unless otherwise noted, the following conditions were used for each specification:

- All filter settings
- All impedance selections
- Sample clock set to 100 MS/s

Typical values are representative of an average unit operating at room temperature. Specifications are subject to change without notice. For the most recent NI 5122 specifications, visit ni.com/manuals.

To access the NI 5122 documentation, including the *NI High-Speed Digitizers Getting Started Guide*, which contains functional descriptions of the NI 5122 signals, navigate to **Start»Programs»National Instruments» NI-SCOPE»Documentation**.



**Caution-Hot Surface** Allow time to cool before extracting NI 5122 hardware from PXI chassis or PC to reduce risk of burns. Exercise caution when handling, as recently used NI 5122 devices may exceed safe handling temperatures.

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## **Vertical**

#### **Analog Input (Channel 0 and Channel 1)**

#### Table 1.

Specification	Va	Comments			
Number of Channels	Two (simultaneously sampled)		Two (simultaneously sampled)		_
Connector	BNC	_			
Impedance and	Coupling				
Input Impedance	50 Ω ±2.0%	1 MΩ ±0.75% in parallel with a typical capacitance of 27 pF ±2 pF	Software selectable		
Input Coupling	AC, DC, GND		AC coupling available on 1 MΩ only		

Table 1. (Continued)

C-asifi astis	Specification Value Comments					
Specification			va	lue		Comments
Voltage Levels						_
Full Scale (FS)		50 Ω			1 ΜΩ	_
Input Range and Programmable Vertical Offset	Range $(V_{pk-pk})$		cal Offset nge (V)	Range (V <sub>pk-pk</sub> )	Vertical Offset Range (V)	
	0.2		±0.1	0.2	±0.1	
	0.4		±0.2	0.4	±0.2	
	1		±0.5	1	±0.5	
	2		±1	2	±1	
	4		±2	4	±2	
	10		_	10	±5	
				20	_	
Maximum Input	50 Ω			1 MΩ		_
Overload	$7 V_{rms}$ with $ Peaks  \le 10 V$			Peaks  ≤ 42 V		
Accuracy						
Resolution	14 bits					_
DC Accuracy (Programmable	Range (V <sub>pk-pk</sub>			$50~\Omega$ and $1$	. ΜΩ	Within ±5 °C of self-calibration
Vertical Offset = 0 V)	0.2, 0.4,	1, 2	±(0.	NI PXI-5122: (0.65% of Input + 1.0 mV)		temperature
		NI PCI-5122: ±(0.65% of Input + 2.0 mV)				
	4, 10		±(0.	65% of Input	t + 8.0 mV)	
	20 (1 MΩ or	nly)	±(0.65% of Input + 10.0 mV)			
Programmable Vertical Offset Accuracy	±0.4% of offset setting				Within ±5 °C of self-calibration temperature	
DC Drift	±(0.057% d	of Input	t + 0.006%	of FS + 100 µ	ιV) per °C	_

Table 1. (Continued)

Specification		V	/alue	Comments
AC Amplitude	50 Ω		1 ΜΩ	Within ±5 °C of
Accuracy	±0.06 dE (±0.7%) at 50		±0.09 dB (±1.0%) at 50 kHz	self-calibration temperature
Crosstalk, Typical	≤-100 dB at 10 M	ſНz		CH 0 to/from CH 1, External Trigger to CH 0 or CH 1
Bandwidth and	Transient Response	e		
Bandwidth (-3 dB)	Range (V <sub>pk-pk</sub> )		$50~\Omega$ and $1~M\Omega$	Filters off  *78 MHz above
	All ranges except 0.2	100 MHz 80 MHz up to 40 °C*		40 °C
	0.2			
Rise/Fall Time, Typical	Range (V <sub>pk-pk</sub> )		$50~\Omega$ and $1~M\Omega$	_
	All ranges except 0.2		3.5 ns	
	0.2		4.2 ns	1
Bandwidth	Noise Filt	er	Antialias Filter	Only one filter
Limit Filters	20 MHz 2-pole Bessel		40 MHz (-6 dB, typical) 35 MHz (-3 dB) 6-pole Chebyshev filter	can be enabled at any given time. The antialias filter is enabled by default.
AC-Coupling Cutoff (-3 dB)	12 Hz			AC coupling available on 1 MΩ only

Table 1. (Continued)

Specification		Comments		
Passband Flatness	Filter Settings	Range (V <sub>pk-pk</sub> )	$50~\Omega$ and $1~M\Omega$	Referenced to 50 kHz
	Filters Off	All ranges except 0.2	±0.4 dB DC to 20 MHz ±1 dB 20 MHz to 50 MHz	
		0.2	±0.4 dB DC to 20 MHz ±1 dB 20 MHz to 40 MHz	
	Antialias Filter On	All ranges	±1.2 dB DC to 16 MHz ±1.6 dB 16 MHz to 32 MHz	

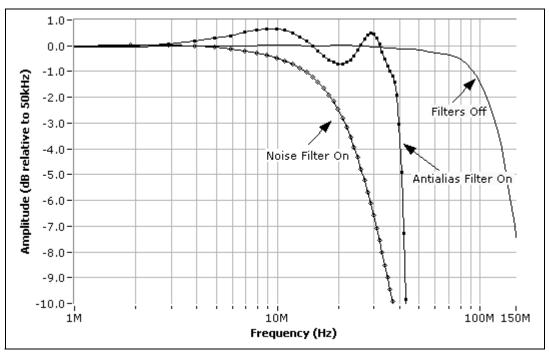


Figure 1. NI 5122 Frequency Response (Typical)

Table 1. (Continued)

Specification		Value		Comments
Spectral Characte	eristics			
Spurious Free Dynamic Range	Range (V <sub>pk-pk</sub> )	50 Ω	1 ΜΩ	10 MHz, -1 dBFS input
with Harmonics (SFDR), Typical	0.2	-75 dBc	–70 dBc	signal.
77 31	0.4	-75 dBc	–70 dBc	Includes the 2nd through
	1	–75 dBc	-70 dBc	the 5th harmonics.  Measured
	2	-75 dBc	–70 dBc	
	4	-65 dBc	–70 dBc	from DC to
	10	-65 dBc	-60 dBc	50 MHz on NI PXI-5122.
	20 (1 MΩ only)	N/A	-60 dBc	Measured from 5 kHz to 50 MHz on NI PCI-5122.

Table 1. (Continued)

Specification Value Comments						
Specification		Value				
Total Harmonic Distortion	Range (V <sub>pk-pk</sub> )	5				10 MHz, -1 dBFS input
(THD), Typical	0.2	-7	5 dBc	-6	8 dBc	signal.
1) prom	0.4	-7	5 dBc	-6	8 dBc	Includes the 2nd through
	1	-7	5 dBc	-6	8 dBc	the 5th harmonics.
	2	-7	3 dBc	-6	8 dBc	narmonics.
	4	-6	3 dBc	-6	8 dBc	
	10	-6	3 dBc	-5	8 dBc	
	20 (1 MΩ only)	]	N/A	-5	8 dBc	
Intermodulation	0.2 V <sub>pl</sub>	<sub>k-pk</sub> to 2.0	V <sub>pk-pk</sub> Range	es on $50\Omega$ l	[nput	Two tones at
Distortion, Typical	-75 dBc					10.2 MHz and 11.2 MHz. Each tone is
						−7 dBFS.
Signal-to-Noise		5	50 Ω	1	ΜΩ	10 MHz,
Ratio (SNR), Typical	Range (V <sub>pk-pk</sub> )	Filters Off	Antialias Filter On	Filters Off	Antialias Filter On	-1 dBFS input signal.
	0.2	60 dB	60 dB	56 dB	60 dB	Excludes harmonics.
	0.4	62 dB	62 dB	61 dB	62 dB	Measured
	1	62 dB	62 dB	62 dB	62 dB	from DC to 50 MHz.
	2	62 dB	62 dB	62 dB	62 dB	JO WILL.
	4		_	61 dB	62 dB	

Table 1. (Continued)

Specification	Value				Comments	
Signal to Noise		4	50 Ω	1	ΜΩ	10 MHz,
and Distortion (SINAD), Typical	$\begin{array}{c} \text{Range} \\ (V_{\text{pk-pk}}) \end{array}$	Filters Off	Antialias Filter On	Filters Off	Antialias Filter On	-1 dBFS input signal.
	0.2	60 dB	60 dB	56 dB	59 dB	Includes harmonics.
	0.4	62 dB	62 dB	60 dB	61 dB	Measured
	1	62 dB	62 dB	61 dB	61 dB	from DC to 50 MHz.
	2	62 dB	62 dB	61 dB	61 dB	JO WIIIZ.
	4	_	_	60 dB	61 dB	

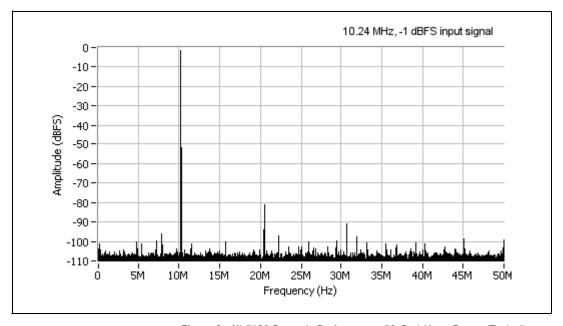


Figure 2. NI 5122 Dynamic Performance, 50  $\Omega,$  1  $\text{V}_{\text{pk-pk}}$  Range (Typical)

Table 1. (Continued)

Specification		Value		Comments
RMS Noise (Noise Filter On)	Range (V <sub>pk-pk</sub> )	50 Ω	1 ΜΩ	50 Ω terminator
	0.2	NI PXI-5122: 46 μV <sub>rms</sub> (0.023% FS)	NI PXI-5122: 60 μV <sub>rms</sub> (0.030% FS)	to input.
		NI PCI-5122: 56 μV <sub>rms</sub> (0.028% FS)	NI PCI-5122: 72 μV <sub>rms</sub> (0.036% FS)	
	0.4	92 μV <sub>rms</sub> (0.023% FS)	$92 \mu V_{rms}$ (0.023% FS)	
	1	230 µV <sub>rms</sub> (0.023% FS)	230 µV <sub>rms</sub> (0.023% FS)	
	2	460 μV <sub>rms</sub> (0.023% FS)	460 μV <sub>rms</sub> (0.023% FS)	
	4	920 μV <sub>rms</sub> (0.023% FS)	920 μV <sub>rms</sub> (0.023% FS)	
	10	2.3 mV <sub>rms</sub> (0.023% FS)	2.3 mV <sub>rms</sub> (0.023% FS)	
	20 (1 MΩ only)	N/A	4.6 mV <sub>rms</sub> (0.023% FS)	

Table 1. (Continued)

Specification		Comments		
RMS Noise (Antialias	Range (V <sub>pk-pk</sub> )	50 Ω	1 ΜΩ	50 Ω terminator
Filter On)	0.2	NI PXI-5122: 66 μV <sub>rms</sub> (0.033% FS)	NI PXI-5122: 80 μV <sub>rms</sub> (0.040% FS)	to input.
		NI PCI-5122: 82 μV <sub>rms</sub> (0.041% FS)	NI PCI-5122: 96 μV <sub>rms</sub> (0.048% FS)	
	0.4	100 μV <sub>rms</sub> (0.025% FS)	120 µV <sub>rms</sub> (0.030% FS)	
	1	250 μV <sub>rms</sub> (0.025% FS)	300 μV <sub>rms</sub> (0.030% FS)	
	2	500 μV <sub>rms</sub> (0.025% FS)	600 μV <sub>rms</sub> (0.030% FS)	
	4	1 mV <sub>rms</sub> (0.025% FS)	1.2 mV <sub>rms</sub> (0.030% FS)	
	10	2.5 mV <sub>rms</sub> (0.025% FS)	3 mV <sub>rms</sub> (0.030% FS)	
	20 (1 MΩ only)	N/A	6 mV <sub>rms</sub> (0.030% FS)	

Table 1. (Continued)

Specification		Comments		
RMS Noise (Filters Off)	Range (V <sub>pk-pk</sub> )	50 Ω	1 ΜΩ	50 Ω terminator
	0.2	NI PXI-5122: 66 μV <sub>rms</sub> (0.033% FS)	NI PXI-5122: 110 μV <sub>rms</sub> (0.055% FS)	to input.
		NI PCI-5122: 90 μV <sub>rms</sub> (0.045% FS)	NI PCI-5122: 110 μV <sub>rms</sub> (0.055% FS)	
	0.4	100 μV <sub>rms</sub> (0.025% FS)	160 μV <sub>rms</sub> (0.040% FS)	
	1	250 µV <sub>rms</sub> (0.025% FS)	300 μV <sub>rms</sub> (0.030% FS)	
	2	500 μV <sub>rms</sub> (0.025% FS)	600 μV <sub>rms</sub> (0.030% FS)	
	4	1 mV <sub>rms</sub> (0.025% FS)	1.6 mV <sub>rms</sub> (0.040% FS)	
	10	2.5 mV <sub>rms</sub> (0.025% FS)	3 mV <sub>rms</sub> (0.030% FS)	
	20 (1 MΩ only)	N/A	6 mV <sub>rms</sub> (0.030% FS)	

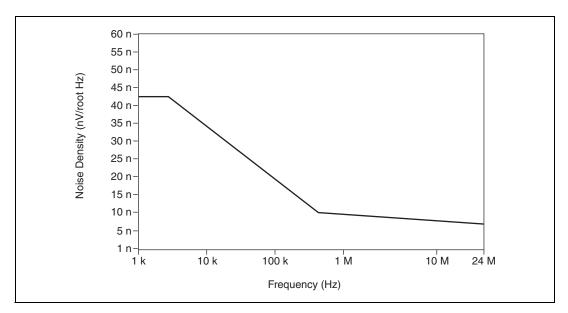


Figure 3. Representation of NI 5122 Spectral Noise Density on 0.2 V Range, Noise Filter Enabled, 1  $M\Omega$  Input Impedance

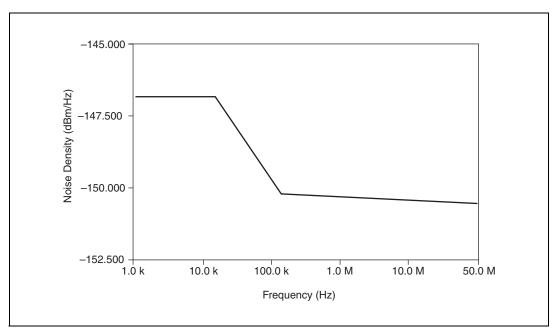


Figure 4. Representation of NI 5122 Spectral Noise Density on 0.2 V Range, Full Bandwidth, 50  $\Omega$  Input Impedance (Does Not Include System Spurs. All Spurs  $\leq$  135 dBm/Hz)

## Horizontal

#### Sample Clock

Table 2.

Specification	Va	lue	Comments
Sources	NI PXI-5122	NI PCI-5122	* Internal Sample
	Internal, Onboard Clock (internal VCXO)*	Internal, Onboard Clock (internal VCXO)*	Clock is locked to the Reference Clock or derived from the
	External, CLK IN (front panel SMB connector)	External, CLK IN (front panel SMB connector)	onboard VCXO.
	External, PXI Star Trigger (backplane connector)		
Onboard Clock (In	nternal VCXO)		
Sample Rate Range	Real-Time Sampling (Single Shot)	Random Interleaved Sampling (RIS)	* Divide by n decimation used
	1.526 kS/s to 100 MS/s*	200 MS/s to 2 GS/s in multiples of 100 MS/s	for all rates less than 100 MS/s. For more information about Sample Clock and decimation, refer to the NI High-Speed Digitizers Help.
Phase Noise Density, Typical	<-100 dBc/Hz at 100 Hz <-120 dBc/Hz at 1 kHz <-130 dBc/Hz at 10 kHz		10 MHz input signal
Sample Clock Jitter, Typical	≤1 ps rms (100 Hz to 100 ≤2 ps rms (100 Hz to 1 M	· · · · · · · · · · · · · · · · · · ·	Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.
Timebase Frequency	100 MHz		_

Table 2. (Continued)

Specification	Va	lue	Comments
Timebase Accuracy	Not Phase-Locked to Reference Clock	Phase-Locked to Reference Clock	_
	±25 ppm	Equal to the Reference Clock accuracy	
Sample Clock Delay Range	±1 Sample Clock period		_
Sample Clock Delay Resolution	10 ps		_
External Sample (	Clock		
Sources	NI PXI-5122	NI PCI-5122	_
	CLK IN (front panel SMB connector)	CLK IN (front panel SMB connector)	
	PXI Star Trigger (backplane connector)		
Frequency Range	30 MHz to 105 MHz		Divide by $n$ decimation available where $1 \le n \le 65,535$ . For more information about Sample Clock and decimation, refer to the $NI$ High-Speed Digitizers Help.
Duty Cycle Tolerance	45% to 55%		_

Table 2. (Continued)

Specification	Value		Comments
Sample Clock Exp	orting		
Exported Sample Clock	Destination	Maximum Frequency	* Decimated Sample Clock only
Destinations	CLK OUT (front panel SMB connector)	105 MHz	
	PXI_Trig <06> (backplane connector)*	20 MHz	
	PFI <01> (front panel 9-pin mini-circular DIN connector)*	25 MHz	
	RTSI<06>*	20 MHz	

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#### Phase-Locked Loop (PLL) Reference Clock

Table 3.

Specification	Va	alue	Comments
Sources	NI PXI-5122	NI PCI-5122	_
	PXI_CLK10 (backplane connector)  CLK IN (front panel SMB connector)	RTSI 7 CLK IN (front panel SMB connector)	
Frequency Range	1 MHz to 20 MHz in 1 MHz increments. Default of 10 MHz.  The PLL Reference Clock frequency has to be accurate to ±50 ppm.		_
Duty Cycle Tolerance	45% to 55%		_
Exported	NI PXI-5122	NI PCI-5122	_
Reference Clock Destinations	CLK OUT (front panel SMB connector)	CLK OUT (front panel SMB connector)	
	PFI <01> (front panel 9-pin mini-circular DIN connector)	PFI <01> (front panel 9-pin mini-circular DIN connector)	
	PXI_Trig <07> (backplane connector)	RTSI <07>	

# **CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)**

Table 4.

Specification	Value	Comments
Input Voltage Range	Sine wave: $0.65~V_{pk-pk}$ to $2.8~V_{pk-pk}$ (0 dBm to 13 dBm) Square wave: $0.2~V_{pk-pk}$ to $2.8~V_{pk-pk}$	_
Maximum Input Overload	7 $V_{rms}$ with $ Peaks  \le 10 \text{ V}$	
Impedance	50 Ω	_
Coupling	AC	_

# **CLK OUT (Sample Clock and Reference Clock Output, Front Panel Connector)**

Table 5.

Specification	Value	Comments
Output Impedance	50 Ω	_
Logic Type	3.3 V CMOS	_
Maximum Drive Current	±48 mA	_

## Trigger

#### Reference (Stop) Trigger

Table 6.

Specification		Va	lue	Comments
Trigger Types		Types	Sources	Refer to the
and Sources	_	indow, Hysteresis, igital, Immediate, ware	CH 0, CH 1, TRIG, PXI_Trig <06>, PFI <01>, PXI Star Trigger, Software, and RTSI <06>	following sections and NI High-Speed Digitizers Help for more information about what sources are available for each trigger type.
Time	TDC	Onboard Clock	External Clock	TDC = Time to
Resolution	On	100 ps	N/A	Digital Conversion
	Off	10 ns	External Clock Period	Circuit
Holdoff	TDC	Onboard Clock	External Clock	_
	On	10 μs to 171.79 s	N/A	
	Off	2 μs to 171.79 s	$200 \times (\text{External Clock})$ Period) to $(2^{32} - 1) \times (\text{External Clock})$ Period)	

Table 6. (Continued)

Specification	Va	llue	Comments
Analog Trigger	r (Edge, Window, and Hyster	esis Trigger Types)	
Sources	CH 0 (front panel BNC connected to the CH 1 (front panel BNC connected to the CH 1) (f	ector)	_
Trigger Level Range	CH 0, CH 1 100% FS	TRIG (External Trigger) ±5 V	_
Trigger Level Resolution	10 bits (1 in 1,024)		_
Edge Trigger Sensitivity	CH 0, CH 1  2.5% FS up to 50 MHz, increasing to 5% FS at 100 MHz	$ \begin{array}{c} TRIG \ (External \ Trigger) \\ \hline 0.25 \ V_{pk\text{-}pk} \ up \ to \ 100 \ MHz, \\ increasing \ to \ 1 \ V_{pk\text{-}pk} \ at \\ 200 \ MHz \end{array} $	_
Level Accuracy, Typical	CH 0, CH 1 ±3.5% FS up to 10 MHz	TRIG (External Trigger)  ±0.35 V (±3.5% FS) up to 10 MHz	_
Jitter	≤80 ps rms		Within ±5 °C of self-calibration temperature
Trigger Filters	Low-Frequency (LF) Reject	High-Frequency (HF) Reject	_
	50 kHz	50 kHz	
Digital Trigger	(Digital Trigger Type)		
Sources	NI PXI-5122	NI PCI-5122	_
	PXI_Trig <06> (backplane connector)  PFI <01> (front panel SMB connector)  PXI Star Trigger (backplane connector)	RTSI <06> PFI <01> (front panel SMB connector)	

Table 6. (Continued)

Specification	Value	Comments	
Video Trigger	Video Trigger (Video Trigger Type)		
Sources	CH 0 (front panel BNC connector)	_	
	CH 1 (front panel BNC connector)		
	TRIG (front panel BNC connector)		
Types	Specific Line	_	
	Any Line		
	Specific Field		
Standard	Negative sync of NTSC, PAL, or SECAM signal	_	

#### TRIG (External Trigger, Front Panel Connector)

Table 7.

Specification	Value	Comments
Connector	BNC	_
Impedance	1 $M\Omega$ in parallel with 22 pF	_
Coupling	AC, DC	_
AC-Coupling Cutoff (-3 dB)	12 Hz	_
Input Voltage Range	±5 V	_
Maximum Input Overload	Peaks  ≤ 42 V	_

# PFI 0 and PFI 1 (Programmable Function Interface, AUX Front Panel Connectors)

Table 8.

Specification	Value	Comments
Connector	9-pin mini-circular DIN	_
Direction	Bi-directional	_
As an Input (Trigge	er)	
Destinations	Start Trigger (Acquisition Arm)	_
	Reference (Stop) Trigger	
	Arm Reference	
	Advance Trigger	
Input Impedance	150 kΩ	_
$V_{IH}$	2.0 V	_
V <sub>IL</sub>	0.8 V	_
Maximum Input Overload	-0.5 V to 5.5 V	_
Maximum Frequency	25 MHz	_
As an Output (Ever	nt)	
Sources	Start Trigger (Acquisition Arm)	_
	Reference (Stop) Trigger	
	End of Record	
	Done (End of Acquisition)	
	Probe Compensation (1 kHz, 50% duty cycle square wave, PFI 1 only)	
Output Impedance	50 Ω	_
Logic Type	3.3 V CMOS	_

Table 8. (Continued)

Specification	Value	Comments
Maximum Drive Current	±24 mA	_
Maximum Frequency	25 MHz	_

## **Waveform Specifications**

Table 9.

Specification	Value		Comments
Onboard Memory Size	8 MB per Channel Standard	4 megasamples per channel	_
	32 MB per Channel Option	16 megasamples per channel	
	256 MB per Channel Option	128 megasamples per channel	
	512 MB per Channel Option	256 megasamples per channel	
Minimum Record Length	1 Sample		_
Number of Pretrigger Samples	Zero up to full Record Length		Single-record mode and multiple-record mode
Number of Posttrigger Samples	Zero up to full Record Length		Single-record mode and multiple-record mode

Table 9. (Continued)

Specification	Value		Comments
Maximum Number of	8 MB per Channel Standard	32,768	_
Records in Onboard Memory	32 MB per Channel Option	131,072	
, and the second	256 MB per Channel Option	1,048,576	
	512 MB per Channel Option	2, 097,152	
Allocated Onboard Memory per Record	Record Length in samples + 100 samples. Round the sum up to the next multiple of 64 samples.  1 sample = 2 bytes		_

## **Calibration**

Table 10.

Specification	Value	Comments
Self-Calibration	Self-calibration is done on software command. The calibration corrects for gain, offset, frequency response, triggering, and timing adjustment errors for all input ranges.	_
External Calibration (Factory Calibration)	The external calibration calibrates the VCXO and the voltage reference. Appropriate constants are stored in nonvolatile memory.	
Interval for External Calibration	2 years	_
Warm-Up Time	15 minutes	_

#### **Power**

Table 11.

Specification	Typical Value		Comments
	NI PXI-5122	NI PCI-5122	_
+3.3 VDC	1.4 A	1.4 A	
+5 VDC	1.5 A	2.4 A	
+12 VDC	110 mA	110 mA	
-12 VDC	270 mA	0 A	
Total Power	16.7 W	17.9 W	

#### Software

Table 12.

Specification	Value	Comments
Driver	NI-SCOPE 2.6 or later	_
Software	NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5122. NI-SCOPE provides application programming interfaces for many development environments.	
Application Software	NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:	_
	• LabVIEW	
	• LabWindows <sup>TM</sup> /CVI <sup>TM</sup>	
	Measurement Studio	
	• Microsoft Visual C/C++	
	Microsoft Visual Basic	
Interactive Soft Front Panel and	The Scope Soft Front Panel 2.0.1 or later supports interactive control of the NI 5122. The Scope Soft Front Panel is included on the NI-SCOPE CD.	_
Configuration	National Instruments Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the NI 5122. MAX is included on the NI-SCOPE CD.	

#### **Environment**

#### NI PXI-5122 Environment



**Note** To ensure that the NI PXI-5122 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included in the NI PXI-5122 kit. The NI PXI-5122 is intended for indoor use only.

Table 13.

Specification	Value	Comments
Operating	0 °C to +55 °C in all NI PXI chassis except the following:	_
Temperature	0 °C to +45 °C when installed in an NI PXI-1000/B or PXI-101x chassis	
	Meets IEC-60068-2-1 and IEC-60068-2-2.	
Storage Temperature	-40 °C to +70 °C. Meets IEC-60068-2-1 and IEC-60068-2-2.	
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC-60068-2-56.	
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC-60068-2-56.	
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	
Operating Vibration	5 Hz to 500 Hz, 0.31 g <sub>rms</sub> . Meets IEC-60068-2-64.	_
Storage Vibration	5 Hz to 500 Hz, 2.46 g <sub>rms</sub> . Meets IEC-60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	
Altitude	2,000 m maximum (at 25 °C ambient temperature)	_
Pollution Degree	2	_

#### NI PCI-5122 Environment



**Note** To ensure that the NI PCI-5122 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included in the NI PCI-5122 kit. Also, to maximize airflow and extend the life of the device, leave any adjacent PCI slots empty. The NI PCI-5122 is intended for indoor use only.

Table 14.

Specification	Value	Comments
Operating Temperature	0 °C to +45 °C. Meets IEC-60068-2-1 and IEC-60068-2-2.	_
Storage Temperature	-40 °C to +70 °C. Meets IEC-60068-2-1 and IEC-60068-2-2.	_
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC-60068-2-56.	_
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC-60068-2-56.	_
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	_
Storage Vibration	5 Hz to 500 Hz, 2.46 g <sub>rms</sub> . Meets IEC-60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	_
Altitude	2,000 m maximum (at 25 °C ambient temperature)	_
Pollution Degree	2	_

# Safety, Electromagnetic Compatibility, and CE Compliance

Table 15.

Specification	Value	Comments		
Safety	The NI 5122 meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:	For UL and other safety certifications, refer to the product label or visit ni.com/certification.		
	• IEC 61010-1, EN 61010-1			
	• UL 61010-1			
	• CAN/CSA-C22.2 No. 61010-1			
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	_		
Immunity	EN 61326:1997 + A2:2001, Table 1	_		
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant.	_		
	For EMC compliance, operate this device with shielded cabling.			
_	This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:			
Low-Voltage Directive (safety)	73/23/EEC	_		
Electromagnetic Compatibility Directive (EMC)	89/336/EEC	_		

Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

#### **Physical**

Table 16.

Specification	Value		Comments
	NI PXI-5122	NI PCI-5122	
Dimensions	Single 3U PXI Slot. CompactPCI compatible	35.5 × 11.3 × 2.0 cm (13.4 × 4.4 × 0.8 in.)	_
Weight	3823 g (13.5 oz.)	455 g (16 oz.)	
Front Panel Co	nnectors		
Label	Function	Connector T	Гуре
CH 0	Analog Input	BNC female	
CH 1	Analog Input	BNC female	
TRIG	External Trigger	BNC female	
CLK IN	Sample Clock Input and Reference Clock Input	SMB jack	
CLK OUT	Sample Clock Output and Reference Clock Output	SMB jack	
AUX I/O	PFI 0, PFI 1 9-pin mini-circular DIN		
NI PXI-5122 Front Panel Indicators			
Label	Function		For more
ACCESS	The ACCESS LED indicates the status of the PCI bus and the interface from the NI PXI-5122 to the controller.		information, refer to the NI High-Speed
ACTIVE	The ACTIVE LED indicates the status of the onboard acquisition hardware of the NI PXI-5122.		Digitizers Help.



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